REMARKS

With this amendment, Claims 1-26 are pending in the present application. Claims 1, 2, and 19 have been amended. The specific amendments made to the claims are shown in the "Version With Markings to Show Changes Made" following the signature page of this amendment, with additions being underlined and deletions [in brackets]. Applicant is also filing herewith a Proposed Drawing Amendment to amend Figure 5 of the drawings. In view of the foregoing amendment and the following remarks, Applicant respectfully requests reconsideration and allowance of this application.

Objections to the drawings

The Examiner objected to the drawings under 37 CFR 1.83(a) because the drawings do not show one of the limitations recited Claim 17. Specifically, the Examiner indicated that the drawings do not show the feature of "a fourth insulating layer formed on the lower surface of the first chip". Applicant has addressed this concern by amending the drawings as specified in the attached PROPOSED DRAWING AMENDMENT. In particular, Applicant has amended Figure 5 to show a fourth insulating layer formed on the lower surface of the first chip. Thus, Applicant submits that the drawings are now in compliance with the informalities noted by the Examiner.

Claim Rejections – 35 U.S.C. § 112

The Examiner rejected Claims 6, 10, and 12 under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the Examiner indicated that the term "approximately" is a relative term which renders the claim indefinite and that the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not reasonably be apprised of the scope of the invention. Applicant respectfully disagrees with the Examiner and submits that one of ordinary skill in the art of semiconductor manufacturing would mostly likely know that there is a standard deviation associated with most, if not all, manufacturing processes and measurement methods. Accordingly, when the term "approximately" is placed before a value or measurement, the skilled artisan clearly understands that the value can range from the target value plus or minus the standard deviation associated with the manufacturing process and/or the measurement process. As such, Applicant respectfully submits that Claims 6, 10, and 12 meet the requirements of 35 U.S.C. § 112, second paragraph.

Claim Rejections – 35 U.S.C. § 103

The Examiner rejected Claims 1-26 under 35 U.S.C. § 103(a) as being unpatentable over Asada in view of Morinaga. However, after carefully reviewing both references, Applicant notes that neither reference teaches or suggests a multichip module having an insulating layer comprised of enclosed regions of air. Furthermore, Applicant submits that there would have been no motivation to combine Asada with Morinaga to form a multichip module having an inter-chip insulating layer with enclosed regions of air dispersed therethrough to reduce capacitive coupling between conductors on adjacent chips. Asada is concerned with reducing the overall height of a multichip module (MCM) and stacking the chips in a manner so that the MCM can better withstand stress and resist cracking. Asada does not at all address the problem associated with capacitive coupling between conductors formed in adjacent chips. In fact, the MCM structure shown in Asada is unlikely to have a significant capacitive coupling problem between conductors in adjacent chips because the adjacent chips are separated by a sufficiently wide distance comprised of the thickness of the insulating layer 601 and a resin layer 621 (*See, e.g.,* Figure 8B of Asada.)

Moreover, it would be counterintuitive to form enclosed regions of air in the insulating substrate described in Asada. According to Asada, the insulating substrate is comprised of a "tape-like insulating polymer film" that is laminated to a copper thin film whereby patterning is carried out so as to delineate plural patterns of the copper wiring on the insulating substrate. (*See, e.g.,* Column 15, Lines 27-54 of Asada) The formation of voids in the insulating substrate is likely to cause the copper wiring to delaminate from the insulating substrate in regions where the voids are present in the interface between the insulating substrate and the metal wiring, which can ultimately cause the module to malfunction. Accordingly, not only does the MCM structure recited in Asada appear not to have a significant capacitive coupling problem that is being addressed by Applicant's invention, the manner in which Applicant's invention is proposing to reduce capacitive coupling can actually be detrimental to the MCM described in Asada. Thus, Applicant respectfully submits there would be no motivation to incorporate the voids in the insulator described in Morinaga to the insulating substrate of the MCM recited in Asada and that the pending claims are patentable over Asada in view of Morinaga.

CONCLUSION

Hence Applicant respectfully submits that the pending claims are allowable over the cited references and the application is now in condition for immediate allowance and requests the prompt allowance of the same. Should there be any impediment to the prompt allowance of this application that could be resolved by a telephone conference, the Examiner is respectfully requested to call the undersigned at the number shown below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 10/7/2002

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Version with Markings to Show Changes Made

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A high density semiconductor structure having a plurality of integrated circuit chips, comprising:

a first integrated circuit chip having an upper bonding surface;

a second integrated circuit chip secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip;

a chip insulating layer disposed between the first and second chips so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material and a plurality of enclosed regions of air dispersed throughout the insulating material, wherein **[the enclosed regions of air causes]** the dielectric constant of the chip insulating layer **[to be]** is less than the dielectric constant of the insulating material.

2. (Amended) The semiconductor structure of Claim 1 further comprises a conductor insulating layer formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material and a plurality of enclosed regions of air dispersed throughout the insulating material, wherein **[the enclosed regions of air causes]** the dielectric constant of the conductor insulating layer **[to be]** is lower than the dielectric constant of the insulating material.

19. (Amended) A multichip cube structure having a plurality of integrated circuit chips, comprising:

a first integrated circuit chip having a first insulating layer disposed on an upper surface of the chip so as to electrically isolate a plurality of metal leads disposed on the upper surface thereof, wherein the first insulating layer is comprised of an insulating material having a first dielectric constant, wherein at least a portion of the first insulating

layer contains enclosed regions of air **[that reduce]**, wherein the dielectric constant of the first insulating layer **[to a value]** is lower than the first dielectric constant;

a second integrated circuit chip secured to the first chip in a manner such that a lower surface of the second chip is positioned adjacent the upper surface of the first chip;

a second insulating layer disposed between the first and second chips wherein the second insulating layer is comprised of a second insulating material having a second dielectric constant, wherein at least a portion of the second insulating layer contains a plurality of enclosed regions of air **[that reduce]**, wherein the dielectric constant of the second insulating layer **[to a value]** is lower than the **[first]** second dielectric constant.

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